Multiple Choice Questions and Answers

1. The _____ format is usually used to store data.

   a) BCD

   b) Decimal

   c) Hexadecimal

   d) Octal

   Answer: a) BCD

2. The 8-bit encoding format used to store data in a computer is _____

   a) ASCII

   b) EBCDIC

   c) ANCI

   d) USCII

   Answer: b) EBCDIC

3. A source program is usually in _____

   a) Assembly language

   b) Machine level language

   c) High-level language

   d) Natural language

Answer: c) High-level language

4. Which memory device is generally made of semiconductors?

   a) RAM

   b) Hard-disk

   c) Floppy disk

   d) Cd disk

   Answer: a) RAM

5. The small extremely fast, RAM's are called as _____

   a) Cache

   b) Heaps

   c) Accumulators

   d) Stacks

   Answer: a) Cache

6. The ALU makes use of _____ to store the intermediate results.

   a) Accumulators

   b) Registers

   c) Heap

   d) Stack

   Answer: a) Accumulators

7. The control unit controls other units by generating _____

a) Control signals

b) Timing signals

c) Transfer signals

d) Command Signals

Answer: b) Timing signals

8. _____ are numbers and encoded characters, generally used as operands.

a) Input

b) Data

c) Information

d) Stored Values

Answer: b) Data

9. The Input devices can send information to the processor.

a) When the SIN status flag is set

b) When the data arrives regardless of the SIN flag

c) Neither of the cases

d) Either of the cases

Answer: a) When the SIN status flag is set

10. _____ bus structure is usually used to connect I/O devices.

    a) Single bus

    b) Multiple bus

    c) Star bus

    d) Rambus

    Answer: a) Single bus

11. The I/O interface required to connect the I/O device to the bus consists of _____

    a) Address decoder and registers

    b) Control circuits

    c) Address decoder, registers and Control circuits

    d) Only Control circuits

    Answer: c) Address decoder, registers and Control circuits

12. To reduce the memory access time we generally make use of _____

    a) Heaps

    b) Higher capacity RAM's

    c) SDRAM's

    d) Cache's

    Answer: d) Cache's

13. _____ is generally used to increase the apparent size of physical memory.

a) Secondary memory

b) Virtual memory

c) Hard-disk

d) Disks

Answer: b) Virtual memory

14. MFC stands for _____

a) Memory Format Caches

b) Memory Function Complete

c) Memory Find Command

d) Mass Format Command

Answer: b) Memory Function Complete

15. The time delay between two successive initiations of memory operation _____

a) Memory access time

b) Memory search time

c) Memory cycle time

d) Instruction delay

Answer: c) Memory cycle time

16. The main virtue of using single Bus structure is _____

a) Fast data transfers

b) Cost effective connectivity and speed

c) Cost effective connectivity and ease of attaching peripheral devices

d) None of the mentioned

Answer: c) Cost effective connectivity and ease of attaching peripheral devices

17. _____ are used to overcome the difference in data transfer speeds of various devices.

a) Speed enhancing circuitory

b) Bridge circuits

c) Multiple Buses

d) Buffer registers

Answer: d) Buffer registers

18. To extend the connectivity of the processor bus we use _____

a) PCI bus

b) SCSI bus

c) Controllers

d) Multiple bus

Answer: a) PCI bus

19. IBM developed a bus standard for their line of computers 'PC AT' called _____

a) IB bus

b) M-bus

c) ISA

d) None of the mentioned

Answer: c) ISA

20. The bus used to connect the monitor to the CPU is _____

a) PCI bus

b) SCSI bus

c) Memory bus

d) Rambus

Answer: b) SCSI bus

21. ANSI stands for _____

a) American National Standards Institute

b) American National Standard Interface

c) American Network Standard Interfacing

d) American Network Security Interrupt

Answer: a) American National Standards Institute

22. _____ register Connected to the Processor bus is a single-way transfer capable.

a) PC

b) IR

c) Temp

d) Z

Answer: d) Z

23. In multiple Bus organisation, the registers are collectively placed and referred as _____

a) Set registers

b) Register file

c) Register Block

d) Map registers

Answer: b) Register file

24. The main advantage of multiple bus organisation over a single bus is _____

a) Reduction in the number of cycles for execution

b) Increase in size of the registers

c) Better Connectivity

d) None of the mentioned

Answer: a) Reduction in the number of cycles for execution

25. The ISA standard Buses are used to connect _____

    a) RAM and processor

    b) GPU and processor

    c) Harddisk and Processor

    d) CD/DVD drives and Processor.

    Answer: c) Harddisk and Processor

26. The decoded instruction is stored in _____

    a) IR

    b) PC

    c) Registers

    d) MDR

    Answer: a) IR

27. The instruction -> Add LOCA, R0 does _____

    a) Adds the value of LOCA to R0 and stores in the temp register

    b) Adds the value of R0 to the address of LOCA

    c) Adds the values of both LOCA and R0 and stores it in R0

    d) Adds the value of LOCA with a value in accumulator and stores it in R0

Answer: c) Adds the values of both LOCA and R0 and stores it in R0

28. Which registers can interact with the secondary storage?

    a) MAR

    b) PC

    c) IR

    d) R0

    Answer: a) MAR

29. During the execution of a program which gets initialized first?

    a) MDR

    b) IR

    c) PC

    d) MAR

    Answer: c) PC

30. Which of the register/s of the processor is/are connected to Memory Bus?

    a) PC

    b) MAR

    c) IR

    d) Both PC and MAR

Answer: b) MAR

31. ISP stands for _____

    a) Instruction Set Processor

    b) Information Standard Processing

    c) Interchange Standard Protocol

    d) Interrupt Service Procedure

    Answer: a) Instruction Set Processor

32. The internal components of the processor are connected by _____

    a) Processor intra-connectivity circuitry

    b) Processor bus

    c) Memory bus

    d) Rambus

    Answer: b) Processor bus

33. _____ is used to choose between incrementing the PC or performing ALU operations.

    a) Conditional codes

    b) Multiplexer

    c) Control unit

d) None of the mentioned

Answer: b) Multiplexer

34. The registers, ALU and the interconnection between them are collectively called as _____

a) process route

b) information trail

c) information path

d) data path

Answer: d) data path

35. _____ is used to store data in registers.

a) D flip flop

b) JK flip flop

c) RS flip flop

d) None of the mentioned

Answer: a) D flip flop

36. During the execution of the instructions, a copy of the instructions is placed in the _____

a) Register

b) RAM

c) System heap

d) Cache

Answer: d) Cache

37. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

a) A

b) B

c) Both take the same time

d) Insufficient information

Answer: a) A

38. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____

a) Super-scaling

b) Pipe-lining

c) Parallel Computation

d) None of the mentioned

Answer: b) Pipe-lining

39. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?

a) ISA

b) ANSA

c) Super-scalar

d) All of the mentioned

Answer: c) Super-scalar

40. The clock rate of the processor can be improved by _____

a) Improving the IC technology of the logic circuits

b) Reducing the amount of processing done in one step

c) By using the overclocking method

d) All of the mentioned

Answer: d) All of the mentioned

41. An optimizing Compiler does _____

a) Better compilation of the given piece of code

b) Takes advantage of the type of processor and reduces its process time

c) Does better memory management

d) None of the mentioned

Answer: b) Takes advantage of the type of processor and reduces its process time

42. The ultimate goal of a compiler is to _____

a) Reduce the clock cycles for a programming task

b) Reduce the size of the object code

c) Be versatile

d) Be able to detect even the smallest of errors

Answer: a) Reduce the clock cycles for a programming task

43. SPEC stands for _____

a) Standard Performance Evaluation Code

b) System Processing Enhancing Code

c) System Performance Evaluation Corporation

d) Standard Processing Enhancement Corporation

Answer: c) System Performance Evaluation Corporation

44. As of 2000, the reference system to find the performance of a system is _____

a) Ultra SPARC 10

b) SUN SPARC

c) SUN II

d) None of the mentioned

Answer: Ultra SPARC 10

45. When Performing a looping operation, the instruction gets stored in the _____

a) Registers

b) Cache

c) System Heap

d) System stack

Answer: b) Cache

46. The average number of steps taken to execute the set of instructions can be made to be less than one by following _____

a) ISA

b) Pipe-lining

c) Super-scaling

d) Sequential

Answer: c) Super-scaling

47. If a processor clock is rated as 1250 million cycles per second, then its clock period is _____

a) 1.9 * 10-10 sec

b) 1.6 * 10-9 sec

c) 1.25 * 10-10 sec

d) 8 * 10-10 sec

Answer: d) 8 * 10-10 sec

48. If the instruction, Add R1, R2, R3 is executed in a system that is pipe-lined, then the value of S is (Where S is a term of the Basic performance equation)?

    a) 3

    b) ~2

    c) ~1

    d) 6

    Answer: c) ~1

49. CISC stands for _____

    a) Complete Instruction Sequential Compilation

    b) Computer Integrated Sequential Compiler

    c) Complex Instruction Set Computer

    d) Complex Instruction Sequential Compilation

    Answer: c) Complex Instruction Set Computer

50. As of 2000, the reference system to find the SPEC rating are built with _____ Processor.

    a) Intel Atom SParc 300Mhz

    b) Ultra SPARC -III 300MHZ

    c) Amd Neutrino series

d) ASUS A series 450 Mhz

Answer: b) Ultra SPARC -III 300MHZ

51. The instruction, Add #45,R1 does _____

a) Adds the value of 45 to the address of R1 and stores 45 in that address

b) Adds 45 to the value of R1 and stores it in R1

c) Finds the memory location 45 and adds that content to that of R1

d) None of the mentioned

Answer: b) Adds 45 to the value of R1 and stores it in R1

52. In the case of, Zero-address instruction method the operands are stored in _____

a) Registers

b) Accumulators

c) Push down stack

d) Cache

Answer: c) Push down stack

53. Add #45, when this instruction is executed the following happen/s _____

a) The processor raises an error and requests for one more operand

b) The value stored in memory location 45 is retrieved and one more operand is requested

c) The value 45 gets added to the value on the stack and is pushed onto the stack

d) None of the mentioned

e) Answer: b) The value stored in memory location 45 is retrieved and one more operand is requested

54. The addressing mode which makes use of in-direction pointers is _____

a) Indirect addressing mode

b) Index addressing mode

c) Relative addressing mode

d) Offset addressing mode

Answer: a) Indirect addressing mode

55. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____

a) EA = 5+R1

b) EA = R1

c) EA = [R1]

d) EA = 5+[R1]

Answer: d) EA = 5+[R1]

56. The addressing mode/s, which uses the PC instead of a general purpose register is _____

a) Indexed with offset

b) Relative

c) Direct

d) Both Indexed with offset and direct

Answer: b) Relative

57. When we use auto increment or auto decrements, which of the following is/are true?

1) In both, the address is used to retrieve the operand and then the address gets altered

2) In auto increment, the operand is retrieved first and then the address altered

3) Both of them can be used on general purpose registers as well as memory locations

a) 1, 2, 3

b) 2

c) 1, 3

d) 2, 3

Answer: d) 2, 3

58. The addressing mode, where you directly specify the operand value is _____

a) Immediate

b) Direct

c) Definite

d) Relative

Answer: a) Immediate

59. The effective address of the following instruction is MUL 5(R1,R2).

a) 5+R1+R2

b) 5+(R1*R2)

c) 5+[R1]+[R2]

d) 5*([R1]+[R2])

Answer: c) 5+[R1]+[R2]

60. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.

a) Relative

b) Indirect

c) Index with Offset

d) Immediate

Answer: a) Relative

61. RTN stands for _____

a) Register Transfer Notation

b) Register Transmission Notation

c) Regular Transmission Notation

d) Regular Transfer Notation

Answer: a) Register Transfer Notation

62. The instruction, Add Loc,R1 in RTN is _____

a) AddSetCC Loc+R1

b) R1=Loc+R1

c) Not possible to write in RTN

d) R1<-[Loc]+[R1]

Answer: d) R1<-[Loc]+[R1]

63. Can you perform an addition on three operands simultaneously in ALN using Add instruction?

a) Yes

b) Not possible using Add, we've to use AddSetCC

c) Not permitted

d) None of the mentioned

Answer: c) Not permitted

64. The instruction, Add R1,R2,R3 in RTN is _____

a) R3=R1+R2+R3

b) R3<-[R1]+[R2]+[R3]

c) R3=[R1]+[R2]

d) R3<-[R1]+[R2]

Answer: d) R3<-[R1]+[R2]

65. In a system, which has 32 registers the register id is _____ long.

a) 16 bit

b) 8 bits

c) 5 bits

d) 6 bits

Answer: c) 5 bits

66. The two phases of executing an instruction are _____

a) Instruction decoding and storage

b) Instruction fetch and instruction execution

c) Instruction execution and storage

d) Instruction fetch and Instruction processing

Answer: b) Instruction fetch and instruction execution

67. The Instruction fetch phase ends with _____

a) Placing the data from the address in MAR into MDR

b) Placing the address of the data into MAR

c) Completing the execution of the data and placing its storage address into MAR

d) Decoding the data in MDR and placing it in IR

Answer: d) Decoding the data in MDR and placing it in IR

68. While using the iterative construct (Branching) in execution _____instruction is used to check the condition.

a) TestAndSet

b) Branch

c) TestCondn

d) None of the mentioned

Answer: b) Branch

69. When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____

a) Branch target

b) Loop target

c) Forward target

d) Jump instruction

Answer: a) Branch target

70. The condition flag Z is set to 1 to indicate _____

a) The operation has resulted in an error

b) The operation requires an interrupt call

c) The result is zero

d) There is no empty register available

Answer: c) The result is zero

71. Which method/s of representation of numbers occupies a large amount of memory than others?

a) Sign-magnitude

b) 1's complement

c) 2's complement

d) 1's & 2's compliment

Answer: a) Sign-magnitude

72. Which representation is most efficient to perform arithmetic operations on the numbers?

a) Sign-magnitude

b) 1's complement

c) 2'S complement

d) None of the mentioned

Answer: c) 2'S complement

73. Which method of representation has two representations for '0'?

a) Sign-magnitude

b) 1's complement

c) 2's complement

d) None of the mentioned

Answer: a) Sign-magnitude

74. When we perform subtraction on -7 and 1 the answer in 2's complement form is _____

a) 1010

b) 1110

c) 0110

d) 1000

Answer: d) 1000

75. When we perform subtraction on -7 and -5 the answer in 2's complement form is _____

a) 11110

b) 1110

c) 1010

d) 0010

Answer: b) 1110

76. When we subtract -3 from 2 , the answer in 2's complement form is _____

a) 0001

b) 1101

c) 0101

d) 1001

Answer: b) 1101

77. The processor keeps track of the results of its operations using flags called _____

a) Conditional code flags

b) Test output flags

c) Type flags

d) None of the mentioned

Answer: a) Conditional code flags

78. The register used to store the flags is called as _____

a) Flag register

b) Status register

c) Test register

d) Log register

Answer: b) Status register

79. The Flag ‘V’ is set to 1 indicates that _____

a) The operation is valid

b) The operation is validated

c) The operation has resulted in an overflow

d) None of the mentioned

Answer: c) The operation has resulted in an overflow

80. In some pipelined systems, a different instruction is used to add to numbers which can affect the flags upon execution. That instruction is _____

a) AddSetCC

b) AddCC

c) Add++

d) SumSetCC

Answer: a) AddSetCC

81. The smallest entity of memory is called _____

a) Cell

b) Block

c) Instance

d) Unit

Answer: a) Cell

82. The collection of the above mentioned entities where data is stored is called _____

a) Block

b) Set

c) Word

d) Byte

Answer: c) Word

83. An 24 bit address generates an address space of _____ locations.

a) 1024

b) 4096

c) 248

d) 16,777,216

Answer: d) 16,777,216

84. If a system is 64 bit machine, then the length of each word will be _____

a) 4 bytes

b) 8 bytes

c) 16 bytes

d) 12 bytes

Answer: b) 8 bytes

85. The type of memory assignment used in Intel processors is _____

a) Little Endian

b) Big Endian

c) Medium Endian

d) None of the mentioned

Answer: a) Little Endian

86. The return address of the Sub-routine is pointed to by _____

a) IR

b) PC

c) MAR

d) Special memory registers

Answer: b) PC

87. The location to return to, from the subroutine is stored in _____

a) TLB

b) PC

c) MAR

d) Link registers

Answer: d) Link registers

88. What is subroutine nesting?

a) Having multiple subroutines in a program

b) Using a linking nest statement to put many subroutines under the same name

c) Having one routine call the other

d) None of the mentioned

Answer: c) Having one routine call the other

89. The order in which the return addresses are generated and used is _____

a) LIFO

b) FIFO

c) Random

d) Highest priority

Answer: a) LIFO

90. In case of nested subroutines the return addresses are stored in _____

a) System heap

b) Special memory buffers

c) Processor stack

d) Registers

Answer: c) Processor stack

91. Add #%01011101,R1 , when this instruction is executed then _____

a) The binary addition between the operands takes place

b) The Numerical value represented by the binary value is added to the value of R1

c) The addition doesn't take place, whereas this is similar to a MOV instruction

d) None of the mentioned

Answer: a) The binary addition between the operands takes place

92. If we want to perform memory or arithmetic operations on data in Hexa-decimal mode then we use _____ symbol before the operand.

a) ~

b) !

c) $

d) *

Answer: c) $

93. When generating physical addresses from a logical address the offset is stored in _____

a) Translation look-aside buffer

b) Relocation register

c) Page table

d) Shift register

Answer: b) Relocation register

94. The technique used to store programs larger than the memory is _____

a) Overlays

b) Extension registers

c) Buffers

d) Both Extension registers and Buffers

Answer: a) Overlays

95. The unit which acts as an intermediate agent between memory and backing store to reduce process time is _____

a) TLB's

b) Registers

c) Page tables

d) Cache

Answer: d) Cache

96. The private work space dedicated to a subroutine is called as _____

a) System heap

b) Reserve

c) Stack frame

d) Allocation

Answer: c) Stack frame

97. If the subroutine exceeds the private space allocated to it then the values are pushed onto _____

a) Stack

b) System heap

c) Reserve Space

d) Stack frame

Answer: a) Stack

98. _____ pointer is used to point to parameters passed or local parameters of the subroutine.

a) Stack pointer

b) Frame pointer

c) Parameter register

d) Log register

Answer: b) Frame pointer

99. The reserved memory or private space of the subroutine gets deallocated when _____

a) The stop instruction is executed by the routine

b) The pointer reaches the end of the space

c) When the routine's return statement is executed

d) None of the mentioned

Answer: c) When the routine's return statement is executed

100. The private space gets allocated to each subroutine when _____

a) The first statement of the routine is executed

b) When the context switch takes place

c) When the routine gets called

d) When the Allocate instruction is executed

Answer: c) When the routine gets called

101. _____ converts the programs written in assembly language into machine instructions.

a) Machine compiler

b) Interpreter

c) Assembler

d) Converter

Answer: c) Assembler

102. The instructions like MOV or ADD are called as _____

a) OP-Code

b) Operators

c) Commands

d) None of the mentioned

Answer: a) OP-Code

103. The alternate way of writing the instruction, ADD #5,R1 is _____

a) ADD [5],[R1];

b) ADDI 5,R1;

c) ADDIME 5,[R1];

d) There is no other way

Answer: b) ADDI 5,R1;

104. Instructions which won't appear in the object program are called as _____

a) Redundant instructions

b) Exceptions

c) Comments

d) Assembler Directives

Answer: d) Assembler Directives

105. The assembler directive EQU, when used in the instruction: Sum EQU 200 does _____

a) Finds the first occurrence of Sum and assigns value 200 to it

b) Replaces every occurrence of Sum with 200

c) Re-assigns the address of Sum by adding 200 to its original address

d) Assigns 200 bytes of memory starting the location of Sum

Answer: b) Replaces every occurrence of Sum with 200

106. The purpose of the ORIGIN directive is _____

a) To indicate the starting position in memory, where the program block is to be stored

b) To indicate the starting of the computation code

c) To indicate the purpose of the code

d) To list the locations of all the registers used

Answer: a) To indicate the starting position in memory, where the program block is to be stored

107. The directive used to perform initialization before the execution of the code is _____

a) Reserve

b) Store

c) Dataword

d) EQU

Answer: c) Dataword

108. _____ directive is used to specify and assign the memory required for the block of code.

a) Allocate

b) Assign

c) Set

d) Reserve

Answer: d) Reserve

109. _____ directive specifies the end of execution of a program.

a) End

b) Return

c) Stop

d) Terminate

Answer: b) Return

110. The last statement of the source program should be _____

a) Stop

b) Return

c) OP

d) End

Answer: d) End

111. When dealing with the branching code the assembler _____

a) Replaces the target with its address

b) Does not replace until the test condition is satisfied

c) Finds the Branch offset and replaces the Branch target with it

d) Replaces the target with the value specified by the DATAWORD directive

Answer: c) Finds the Branch offset and replaces the Branch target with it

112. The assembler stores all the names and their corresponding values in _____

a) Special purpose Register

b) Symbol Table

c) Value map Set

d) None of the mentioned

Answer: b) Symbol Table

113. The assembler stores the object code in _____

a) Main memory

b) Cache

c) RAM

d) Magnetic disk

Answer: d) Magnetic disk

114. The utility program used to bring the object code into memory for execution is _____

a) Loader

b) Fetcher

c) Extractor

d) Linker

Answer: a) Loader

115. To overcome the problems of the assembler in dealing with branching code we use _____

a) Interpreter

b) Debugger

c) Op-Assembler

d) Two-pass assembler

Answer: d) Two-pass assembler

116. When using the Big Endian assignment to store a number, the sign bit of the number is stored in _____

a) The higher order byte of the word

b) The lower order byte of the word

c) Can't say

d) None of the mentioned

Answer: a) The higher order byte of the word

117. To get the physical address from the logical address generated by CPU we use _____

a) MAR

b) MMU

c) Overlays

d) TLB

Answer: b) MMU

118. _____ method is used to map logical addresses of variable length onto physical memory.

a) Paging

b) Overlays

c) Segmentation

d) Paging with segmentation

Answer: c) Segmentation

119. During the transfer of data between the processor and memory we use _____

a) Cache

b) TLB

c) Buffers

d) Registers

Answer: d) Registers

120. Physical memory is divided into sets of finite size called as _____

a) Frames

b) Pages

c) Blocks

d) Vectors

Answer: a) Frames

121. The appropriate return addresses are obtained with the help of ____ in case of nested routines.

a) MAR

b) MDR

c) Buffers

d) Stack-pointers

Answer: d) Stack-pointers

122. When parameters are being passed on to the subroutines they are stored in _____

a) Registers

b) Memory locations

c) Processor stacks

d) All of the mentioned

Answer: d) All of the mentioned

123. The most efficient way of handling parameter passing is by using _____

a) General purpose registers

b) Stacks

c) Memory locations

d) None of the mentioned

Answer: a) General purpose registers

124. The most Flexible way of logging the return addresses of the subroutines is by using _____

a) Registers

b) Stacks

c) Memory locations

d) None of the mentioned

Answer: b) Stacks

125. The wrong statement/s regarding interrupts and subroutines among the following is/are _____

I. The sub-routine and interrupts have a return statement

II. Both of them alter the content of the PC

III. Both are software oriented

IV. Both can be initiated by the user

a) i, ii and iv

b) ii and iii

c) iv

d) iii and iv

Answer: d) iii and iv